



Amitava Chatterjee, Ph.D.

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BIOGRAPHY

Amitava is a Technical Advisor at Slater Matsil who has in-depth knowledge of semiconductor physics and extensive experience in silicon CMOS technology. From 1985 to 2012 he was an individual contributor at Texas Instruments (TI) performing research on transistor and isolation scaling, latchup prevention, on-chip electrostatic discharge protection, proprietary compact models for analog circuit design, and process integration of I/O transistors, drain-extended MOSFETs, thyristors, bandgap reference bipolars, and passives for digital and analog technology platforms. Amitava's contributions include innovations for TI's first shallow trench isolation technology, the industry's first demonstration of replacement gate CMOS, and core transistor design and process integration for TI's 65 nm low-power platform used in prototype samples to Nokia for the world's first 65 nm phone call.

During 2013 Amitava was PDF Fellow at PDF Solutions where he was an engineering consultant to Globalfoundries for development and yield improvement of 22 nm planar CMOS and 14 nm FinFET technology nodes. He was Lecturer and Senior Lecturer at University of Texas at Dallas, Electrical Engineering Department during 2014 - 2016. He is currently a Visiting Scholar at the Materials Science and Engineering Department of UTD, and affiliated with Plano Senior High School as a tutor in their Advancement via Individual Determination (AVID) tutoring program.

EDUCATION

B.Tech. (Hons.), Electronics and Electrical Communication Engineering,
Indian Institute of Technology, Kharagpur

M.S., Electrical Engineering, Louisiana State University

Ph.D., Electrical Engineering, Rensselaer Polytechnic Institute

ADMISSIONS & HONORS

He is an inventor on 98 US patents, several of which received patent incentive awards for his inventions. Examples of patents include:

- US 6,413,824 – low-cost halo-free transistors in a flow using halo in core CMOS · US 5,909,628 – dummy active for planarity of shallow trench isolation (STI) oxide · US 6,313,010 – high-density plasma (HDP-CVD) oxide for STI trench-fill dielectric · US 5,907,462 US 5,539,233, US 5,465,189, US 4,896,243 – various ESD protection schemes
- Elected to Institute of Electrical and Electronics Engineers (IEEE) Fellow (2010), Citation: “For contributions to complementary metal oxide semiconductor device technology and on-chip electrostatic discharge protection.”
- Elected to Texas Instruments Fellow (2006), Citation: “For his contributions to CMOS process integration, electrostatic discharge protection, and semiconductor device modeling.”
- IEEE Electron Device Letters: Editor-in-Chief, (2012 -2015), Associate Editor, (2001 - 2010)
- IEEE Transactions on Electron Devices: Guest Editor, special issue on “Device Integration Technology for RF and Mixed-Signal SOC,” (March, 2003)
- IEEE International Electron Device Meeting: Subcommittee on CMOS Devices (1999 - 2000)
- SPIE Microelectronics Device Technology Conference:-Program Committee (1997 - 1999)

ARTICLES & PRESENTATIONS

Amitava has co-authored 82 journal and conference papers including seven invited papers and two contributed papers demonstrating the first replacement gate transistors:

1. A. Chatterjee, R.A. Chapman, G. Dixit, J. Kuehne, S. Hattangady, H. Yang, G.A. Brown, R. Aggarwal, U. Erdogan, Q. He, M. Hanratty, D. Rogers, S. Murtaza, SJ Fang, R. Kraft, ALP Rotondaro, JC Hu, M. Terry, W Lee, C. Fernando, A. Konecni, G. Wells, D. Frystak, C. Bowen, M. Rodder, and I-C Chen, “Sub-100nm gate length metal gate NMOS transistors fabricated by a replacement gate process,” International Electron Device Meeting Tech. Dig., pp. 821-824, 1997.
2. A. Chatterjee R.A. Chapman, K. Joyner, M. Otobe, S. Hattangady, M. Bevan, G.A. Brown, H. Yang, Q. He, D. Rogers, S.J. Fang, R. Kraft, A.L.P. Rotondaro, M. Terry, K. Brennan, S-W Aur, J.C. Hu, H.L. Tsai, P. Jones, G. Wilk, M. Aoki, M. Rodder, and I-C Chen, “CMOS Metal Replacement Gate Transistors using Tantalum Pentoxide Gate Insulator,” International Electron Device Meeting Tech. Dig., pp. 777-780, 1998